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Grounding Microstrip Lines With Via Holes

Daniel G. Swanson, Jr.

Abstract—**Grounding microstrip circuits with via holes is an established technology and modeling isolated via holes with analytical models is well known. However, the availability of electromagnetic field solvers provides an opportunity to model via holes and the metalization surrounding them in a more realistic fashion. Calculated equivalent inductances for single and double via hole configurations are presented. A microstrip interdigital filter with grounded resonators provides experimental verification.**

I. Introduction

Most thin film fabrication facilities have a via hole process available to microwave component designers. In most cases the designer will choose the minimum via hole diameter and spacing allowed by the process. Earlier work [1] has focused on analytical models for a single via hole as a function of hole diameter and substrate thickness. But the actual via hole configuration used by the designer is often a more complex combination of several via holes and other microstrip discontinuities. And the significant interactions between several discontinuities in close proximity cannot be accurately described by combining analytical models for isolated elements. In this work, an electromagnetic field solver has been used to compute the equivalent inductance of two different via hole topologies as a function of frequency, substrate thickness and a microstrip discontinuity variable.

II. Single Via Holes

Fig. 1 is the preferred geometry for a single via hole in alumina at Watkins-Johnson. The 13 mil diameter hole is used in both 15 mil thick and 25 mil thick alumina. The surrounding metalization is 24 mils square. A microstrip line of width w could then be connected to one side of square. Because the component designer is most likely to use the minimum via hole diameter and metalization area allowed, the equivalent inductance of this structure can be computed as a function of only line width and frequency. The equivalent inductance is computed at a reference plane defined by the junction of the microstrip line and the square pad around the via hole. For lines other than 24 mils wide it is clear that the model includes a step junction, the inductance of the via hole and the capacitance of the pad surrounding the via.

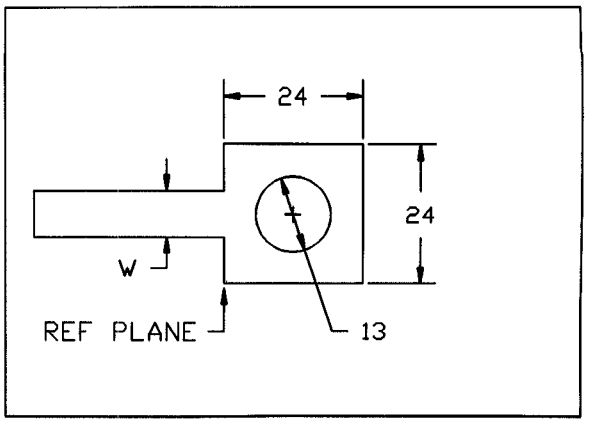

Fig. 1. Microstrip single via hole and microstrip line of width w. All dimensions are mils.

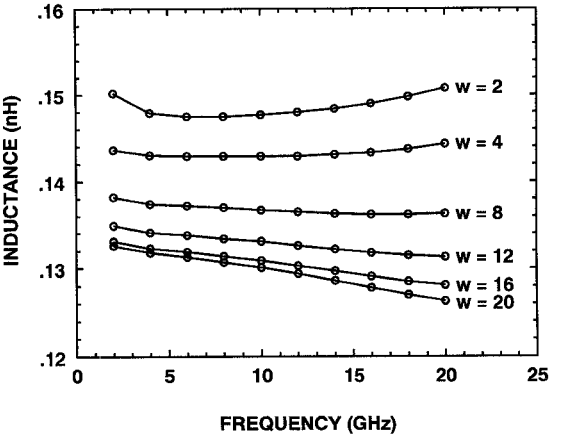

Fig. 2. Equivalent inductance of microstrip single via, alumina substrate, h = 15 mil, ϵ_r = 9.8, w = line width in mils.

The analysis of this structure was carried out on a full wave field solver [2] for several line widths over the 2 to 20 GHz frequency range. The round via hole was approximated by an octagonal hole in the analysis. The results of this analysis for 15 mil thick alumina, ϵ_r = 9.8 are shown in Fig. 2. A similar analysis for 25 mil thick alumina, ϵ_r = 9.8 was also performed with the results shown in Fig. 3. These graphs provide a convenient look-up table for the designer using single via holes.

III. Double Via Holes

Double via holes are often used to decrease the parasitic inductance of the ground connection or to ground a wider microstrip line. Fig. 4 is the preferred geometry for double via holes at Watkins-

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The author is with Watkins-Johnson Company, 3333 Hillview Ave., Stanford Research Park, Palo Alto, CA 94304-1204.
IEEE Log Number 9200862.

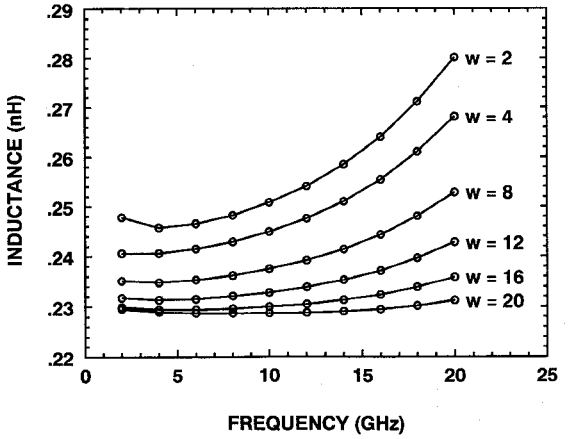

Fig. 3. Equivalent inductance of microstrip single via, alumina substrate, h = 25 mil, ϵ_r = 9.8, w = line width in mils.

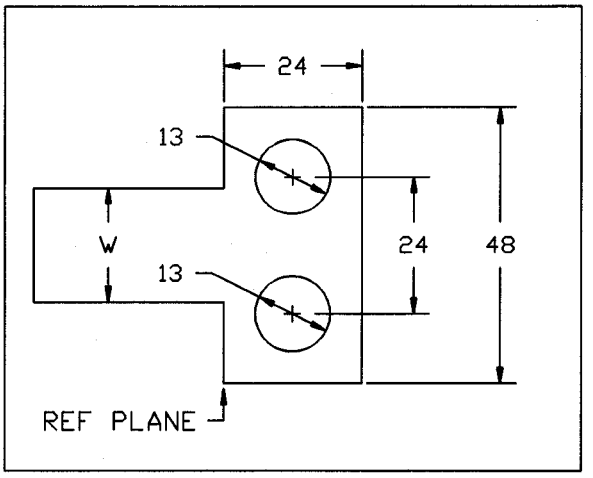

Fig. 4. Microstrip double via holes and microstrip line of width w. All dimensions are mils.

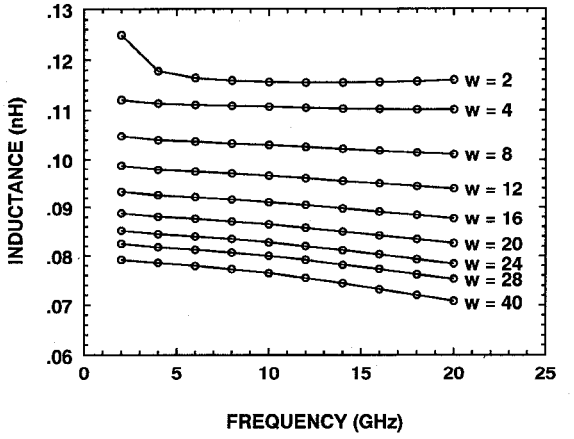

Fig. 5. Equivalent inductance of microstrip double via, alumina substrate, h = 15 mil, ϵ_r = 9.8, w = line width in mils.

Johnson. The two 13 mil diameter via holes are separated by 24 mils center to center. The surrounding metalization is 24 mils by 48 mils. This structure was also analyzed for various line widths over the 2 to 20 GHz frequency range. The results of this analysis for 15 mil thick alumina, ϵ_r = 9.8 are shown in Fig. 5. A similar

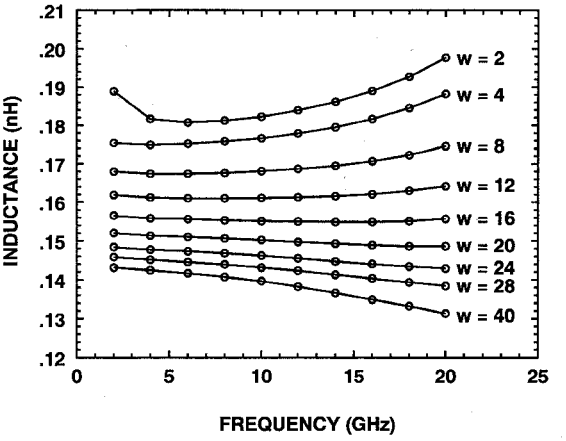

Fig. 6. Equivalent inductance of microstrip double via, alumina substrate, h = 25 mil, ϵ_r = 9.8, w = line width in mils.

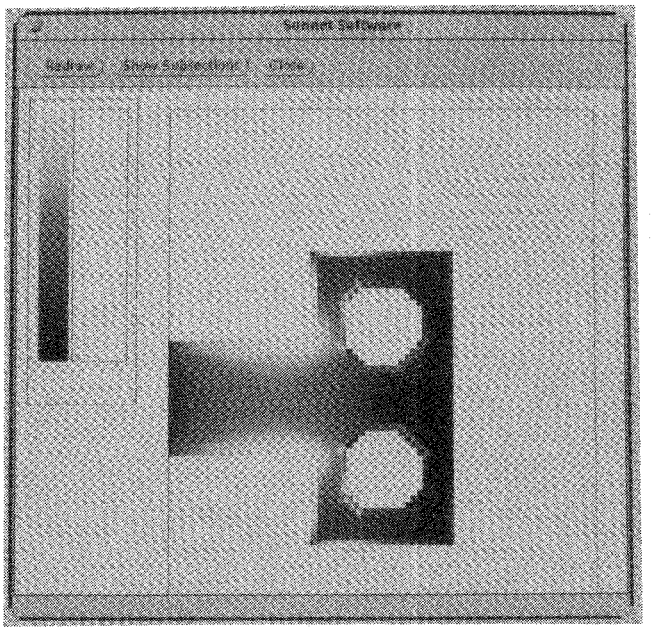

Fig. 7. Current density on microstrip double via, alumina substrate, h = 15 mil, ϵ_r = 9.8, w = 20 mil, freq = 18 GHz.

analysis for 25 mil thick alumina, ϵ_r = 9.8 was also performed with the results shown in Fig. 6.

Note that for both substrate thicknesses the equivalent inductance is lower for the double via holes compared to the single via hole although the ratio is less than two due to the mutual coupling between the double via holes. Also, the dispersion in the equivalent inductance is much higher for the thicker substrates at high frequencies. The sharp increase in equivalent inductance for w = 2 at 2 GHz in all four inductance versus frequency plots is thought to be a numerical precision problem in the analysis.

It is also interesting to observe the conduction current density on the metalization for the double via configuration (Fig. 7). Lightly shaded areas indicate high currents while dark regions indicate low currents. The high current density at the edges of the microstrip line can clearly be seen. The current down the vias follows the shortest path and flows mostly on the sides of the vias nearest the step discontinuity. It may be surprising to some workers that the sides of the via holes away from the step junction and the trailing edge of the surrounding metallization conduct very little current.

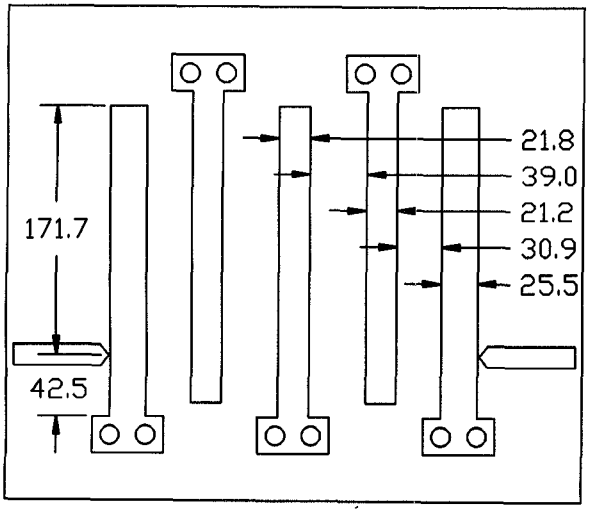

Fig. 8. Microstrip interdigital filter, alumina substrate, $h = 15$ mil, $\epsilon_r = 9.8$. All dimensions are mils.

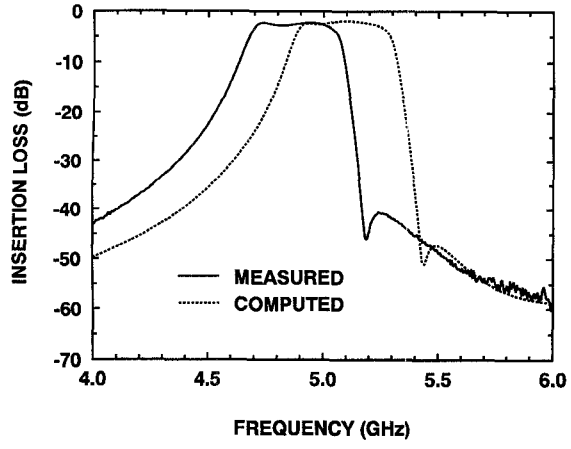

Fig. 9. Measured and computed insertion loss for the microstrip interdigital filter. The parasitic inductance of the via holes was ignored in the design procedure.

There is a high current density on the leading edge of the step and part way down the sides of the via hole pad. But at the outer corners of the step there are very definite current nulls. This distribution of current around the step discontinuity is consistent with computations made by others [3].

Clearly the electromagnetic field solver can account for the nonuniform current distribution on the via holes and their surrounding metalization. In fact, this current distribution will change depending on the exact circuit topology, an effect that would be very difficult to include in a general purpose analytical model.

IV. Experimental Verification

To verify the accuracy of the computations a microstrip interdigital filter was designed and fabricated. The interdigital filter (Fig. 8) is an excellent test case because the center frequency of the fabricated filter is very sensitive to the parasitic inductance of the via hole grounding, and frequency is an easy parameter to measure. The filter was designed assuming the equivalent inductance at the edge of the via pad was zero. The adjacent and non-adjacent couplings between interdigital resonators were modeled using a spectral domain based multi-strip model [4].

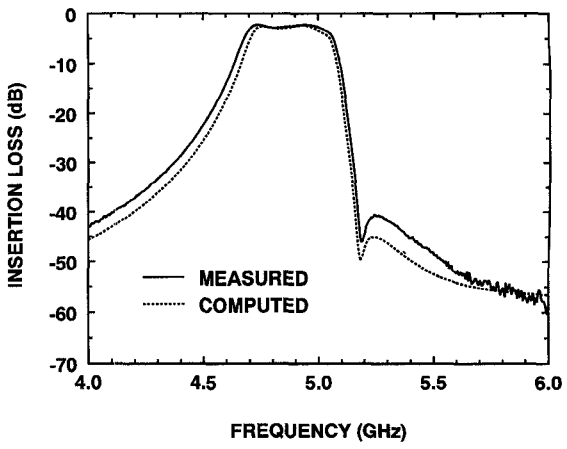

Fig. 10. Measured and computed insertion loss for the microstrip interdigital filter. The computer analysis includes equivalent double via hole inductances from Fig. 5.

The measured versus computed results (assuming zero inductance for the vias) for the filter are shown in Fig. 9. The error in center frequency is approximately 200 MHz or about 4% of the desired center frequency. A second computer prediction was made using the equivalent double via hole inductances from Fig. 5. The measured versus computed results (with via hole inductance) are shown in Fig. 10.

Note the close agreement between the measured and computed center frequencies in Fig. 10. Figs. 9 and 10 together demonstrate the sensitivity of the interdigital filter to the via hole inductance. Fig. 10 demonstrates, at least indirectly, the accuracy of the equivalent inductance values taken from Fig. 5. Similar results for interdigital filters have been achieved at 8 GHz and 14 GHz.

V. Conclusion

Grounding microwave circuits with via holes is an accepted practice. Analytical models for isolated via holes are available but may not fully describe the actual topology. The equivalent inductance of a single via hole or several via holes and their surrounding metalization can be accurately modeled using a full wave electromagnetic field solver. A simple equivalent inductance can be computed directly from the Z-parameters provided by the field solver. A lumped element model with several inductors and capacitors would eliminate the frequency variable and is a more convenient representation for general purpose CAD programs. We are currently working on fitting the computed data to a lumped element model.

A microstrip interdigital filter was designed and built to experimentally verify the computed equivalent inductances. When the parasitic grounding inductances were included in the analysis, the agreement between the computed and measured center frequencies was excellent.

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